## AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A switching circuit comprising:

switching transistors commonly connected to a connection node used as one of a high frequency signal input terminal and a high frequency signal output terminal of the switching circuit; and

a control bias supply circuit that supplies a control bias for cutting off all the switching transistors to one of a source and a drain of each of the switching transistors in order to prevent high frequency signal from substantially propagating through all the switching transistors when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied to gates of all the switching transistors,

wherein the control bias supply circuit comprises a diode having an anode to which a voltage signal is applied from outside of the switching circuit and having a cathode via which the control bias is output in accordance with the voltage signal.

Claims 2-4 (Canceled)

Claim 5 (Currently Amended): ~~The switching circuit as claimed in claim 1,~~ A switching circuit comprising:

switching transistors commonly connected to a connection node used as one of a high frequency signal input terminal and a high frequency signal output terminal of the switching circuit and

a control bias supply circuit that supplies a control bias for cutting off all the switching transistors to one of a source and a drain of each of the switching transistors in order to prevent high frequency signal from substantially propagating through all the switching transistors when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied to gates of all the switching transistors, wherein:

the control bias supply circuit comprises a bias transistor including a structure of a MESFET (metal semiconductor field effect transistor); and

the MESFET having a gate receiving a voltage signal, a first terminal connected to a given potential via a capacitive element, and a second terminal connected to the connection node~~, the control bias being supplied to the connection node from the second terminal~~.

Claim 6 (Previously Presented): The switching circuit as claimed in claim 5, wherein one of a source and a drain of the bias transistor is connected to the connection node via which the

switching transistors are commonly connected, while the other one of the source and drain is connected to a ground potential through a capacitive element.

Claim 7 (Original): The switching circuit as claimed in claim 1, wherein the control bias supply circuit varies a voltage value of the control bias.

Claim 8 (Previously Presented): The switching circuit as claimed in claim 1, wherein the control bias supply circuit selectively supplies one control bias voltage from among a plurality of control bias voltages.

Claim 9 (Original): The switching circuit as claimed in claim 1, wherein the control bias supply circuit varies a voltage value of the control bias when all the switching circuits are in the non-selected state.

Claim10 (Original): The switching circuit as claimed in claim 1, wherein the control bias supply circuit supplies the control bias having a first value when at least one of the switching transistors is in a selected state, and supplies the control bias having a second value different from the first value when all the switching transistors are in the non-selected state.

Claim 11.(Original): The switching circuit as claimed in claim 1, further comprising at least three switching transistors, which are commonly connected to one of the input terminal and the output terminal of the switching circuit.

Claim 12.(Previously Presented): The switching circuit as claimed in claim 1, further comprising shunt transistors respectively provided for the switching transistors and are connected between the connection node and a given potential, gates of the shut transistors receiving the select control signals.

Claim 13 (Original): The switching circuit as claimed in claim 1, wherein the switching transistors are MESFETs.

Claim 14 (Previously Presented): The switching circuit as claimed in claim 1, wherein the common connection node is connected to a ground potential through a resistor.

Claim 15 (Original): The switching circuit as claimed in claim 1, further comprising ballast resistors, each of which is connected between a source and a drain of a corresponding one of the switching transistors.

Claim 16 (Withdrawn): A switching module comprising:

a switching circuit including switching transistors commonly connected to a connection node, and a control bias supply circuit that supplies a control bias for cuffing off all the switching transistors to the switching transistors in order to prevent high frequency signal from substantially propagating through all the switching transistors when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied thereto; and

a decoding circuit that decodes a data signal inputted from an outside of the switching module and produces the selection control signals.

Claim 17 (Withdrawn): The switching module as claimed in claim 16, wherein the switching circuit and the decoding circuit are formed on a single chip.

Claim 18 (Currently Amended): A method of controlling a switching circuit including switching transistors commonly connected to a connection node used as one of a high frequency signal input terminal and a high frequency signal output terminal of the switching circuit, comprising a step of:

supplying a control bias for cutting off all the switching transistors to one of a source and a drain of each of the switching transistors <u>via a diode</u> in order to prevent high frequency signal from substantially propagating through all the switching transistors when all of

the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied to gates of all the switching transistors,

wherein the diode has an anode to which a votage signal is applied from outside of the switching circuit, and a cathode via which the control bias is output in accordance with the voltage signal.

Claim 19 (Original): The method as claimed in claim 18, wherein the step supplies the control bias to the switching transistors in accordance with a voltage signal applied to a gate of a bias transistor that includes a MESFET.

Claim 20 (Original): The method as claimed in claim 18, wherein the step comprises a step of varying a voltage value of the control bias.

Claim 21 (Original): The method of controlling a switching circuit as claimed in claim 18, wherein the step comprises a step of varying a voltage value of the control bias when all the switching transistors are in the non-selected state.

Claim 22 (Original): The method of controlling a switching circuit as claimed in claim 18, wherein the step comprises a step of supplying the control bias having a first voltage value when at least one of the switching transistors is in a selected state and supplying the control bias having a second voltage value different from the first voltage value when all the switching transistors are in the non-selected state.

Claim 23 (New): The switching circuit as claim 1, wherein the control bias is output to the connection node.